IN THE CLAIMS

1. (Currently Amended) A method for forming a semiconductor package, comprising:

providing a substrate having a chip mounted thereon, the substrate having an upper surface and a lower surface opposite the upper surface, the chip being electrically connected to the upper surface of the substrate~~, the substrate having a chip mounted thereon~~;

forming a plurality of void pads on the back surface of the chip, the ~~voids~~ void pads being formed of a material that is non-wettable by solder;

applying a flux on the back surface of the chip, the flux including a solvent;

~~forming~~ arranging a solder preform on the flux; and

reflowing the solder preform to form voids aligned with the void pads.

2. (Original) The method of claim 1, further comprising putting a lid on the solder preform.

3. (Currently Amended) The ~~semiconductor package of any~~ method of claim 1, wherein the voids are formed along a perimeter of the chip at uniform distances from each other.

4. (Original) The method of claim 1, wherein a copper pattern layer is formed on the back surface of the chip to expose the void pads, and wherein a nickel/gold plating layer is formed on the copper pattern layer.

5. (New) A method for forming a semiconductor package, comprising:

providing a substrate having an upper surface and a lower surface opposite the upper surface;

providing a chip mounted to the upper surface of the substrate and electrically connected to the upper surface of the substrate;

forming a plurality of void pads on the back surface of the chip, the void pads being formed of a material that is non-wettable by solder;

applying a flux on the back surface of the chip, the flux including a solvent;

arranging a solder preform on the flux; and

reflowing the solder preform to form voids in the solder preform, wherein the voids are aligned with the void pads.

6. (New) A method for forming a semiconductor package, comprising:

providing a substrate having an upper surface and a lower surface opposite the upper surface;

providing a chip mounted to the upper surface of the substrate and electrically connected to the upper surface of the substrate;

forming a plurality of void pads on the back surface of the chip, the void pads being formed of a material that is non-wettable by a thermal interface material;

forming a conductive pattern layer on the back surface of the chip, wherein the void pads are left exposed on the back surface of the chip;

forming a plating layer on the conductive pattern layer;

applying a flux on the back surface of the chip, the flux including a solvent;

forming a thermal interface material on the flux;

coupling a lid to the thermal interface material; and

reflowing the thermal interface material to form voids in the thermal interface material, wherein the voids are aligned with the void pads.

7. (New) The method of claim 6, wherein the conductive pattern layer comprises copper.

8. (New) The method of claim 6, wherein the plating layer comprises nickel and gold.